Dual Digitally Programmable Potentiometer (DPP™) with 256 Taps and Microwire Interface

FEATURES

- **Two 8-bit DPPs configured as programmable voltage sources in DAC-like applications**
- **Common reference inputs**
- **Non-volatile NVRAM memory wiper storage**
- **Output voltage range includes both supply rails**
- **2 independently addressable buffered output wipers**
- **1 LSB accuracy, high resolution**
- **Serial microwire-like interface**
- **Single supply operation: 2.7V - 5.5V**
- **Setting read-back without effecting outputs**

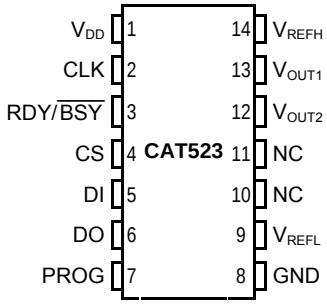
For Ordering Information details, see page 14.

APPLICATIONS

- **Automated product calibration.**
- **Remote control adjustment of equipment**
- **Offset, gain and zero adjustments in self-calibrating and adaptive control systems.**
- **Tamper-proof calibrations.**
- **DAC (with memory) substitute**

PIN CONFIGURATION

PDIP 14-Lead (L)
SOIC 14-Lead (W)



DESCRIPTION

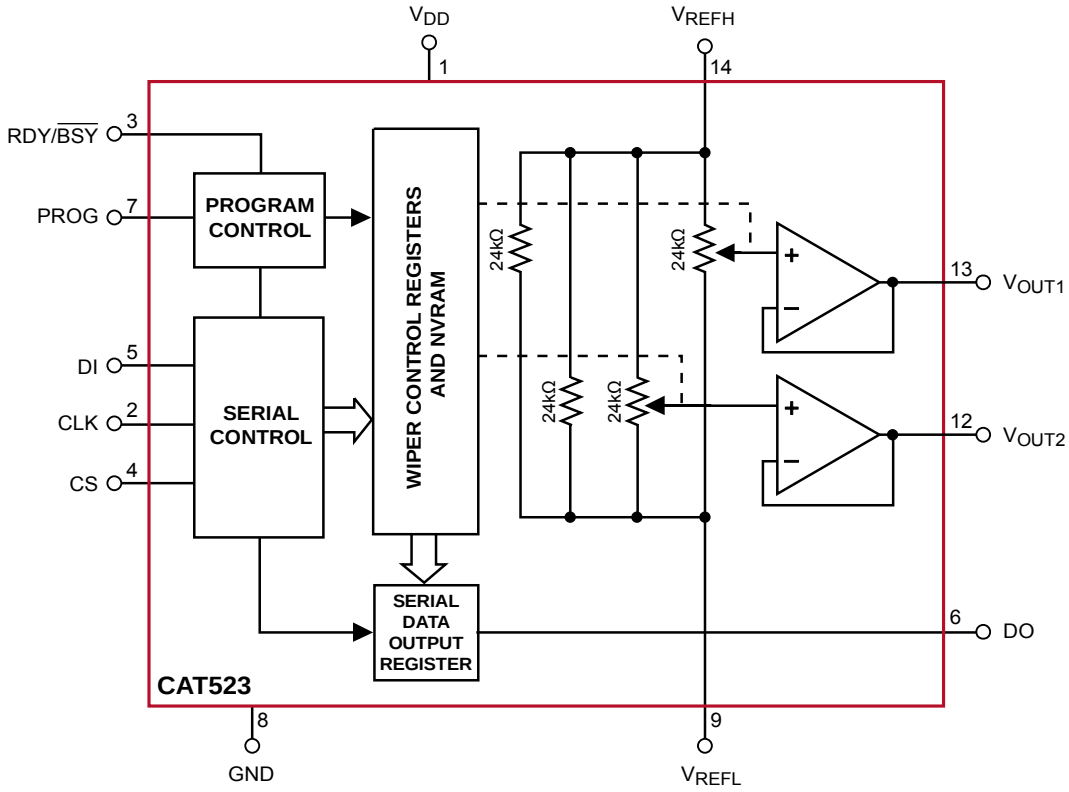
The CAT523 is a dual, 8-bit digitally-programmable potentiometer (DPP™) configured for programmable voltage and DAC-like applications. Intended for final calibration of products such as camcorders, fax machines and cellular telephones on automated high volume production lines, it is also well suited for systems capable of self calibration, and applications where equipment which is either difficult to access or in a hazardous environment, requires periodic adjustment.

The two independently programmable DPPs have a common output voltage range which includes both supply rails. The wipers are buffered by rail to rail op amps. Wiper settings, stored in non-volatile NVRAM memory, are not lost when the device is powered down and are automatically reinstated when power is returned. Each wiper can be dithered to test new output values without effecting the stored settings and stored settings can be read back without disturbing the DPP's output.

Control of the CAT523 is accomplished with a simple 3-wire, Microwire-like serial interface. A Chip Select pin allows several CAT523's to share a common serial interface and communication back to the host controller is via a single serial data line thanks to the CAT523's Tri-Stated Data Output pin. A RDY/$\overline{BSY}$ output working in concert with an internal low voltage detector signals proper operation of non-volatile NVRAM memory Erase/Write cycle.

The CAT523 is available in the 0°C to 70°C Commercial and -40°C to + 85°C Industrial operating temperature ranges and offered in 14-pin plastic DIP and SOIC mount packages.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Parameters	Ratings	Units
Supply Voltage[1]		
V_{DD} to GND	-0.5 to +7	V
Inputs		
CLK to GND	-0.5 to V_{DD} +0.5	V
CS to GND	-0.5 to V_{DD} +0.5	V
DI to GND	-0.5 to V_{DD} +0.5	V
RDY/$\overline{BSY}$ to GND	-0.5 to V_{DD} +0.5	V
PROG to GND	-0.5 to V_{DD} +0.5	V
V_{REFH} to GND	-0.5 to V_{DD} +0.5	V
V_{REFL} to GND	-0.5 to V_{DD} +0.5	V

Parameters	Ratings	Units
Outputs		
D_0 to GND	-0.5 to V_{DD} +0.5	V
V_{OUT} 1– 4 to GND	-0.5 to V_{DD} +0.5	V
Operating Ambient Temperature		
Commercial ('C' or Blank suffix)	0 to +70	°C
Industrial ('I' suffix)	-40 to +85	°C
Junction Temperature	+150	°C
Storage Temperature	-65 to +150	°C
Lead Soldering (10 sec max)	+300	°C

RELIABILITY CHARACTERISTICS

Symbol	Parameter	Test Method	Min	Max	Units
V_{ZAP}[2]	ESD Susceptibility	MIL-STD-883, Test Method 3015	2000		V
I_{LTH}[2][3]	Latch-Up	JEDEC Standard 17	100		mA

POWER SUPPLY

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{DD1}	Supply Current (Read)	Normal Operating	—	400	600	µA
I_{DD2}	Supply Current (Write)	Programming, V_{DD} = 5V	—	1600	2500	µA
		V_{DD} = 3V	—	1000	1600	µA
V_{DD}	Operating Voltage Range		2.7	—	5.5	V

LOGIC INPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
I_{IH}	Input Leakage Current	V_{IN} = V_{DD}	—	—	10	µA
I_{IL}	Input Leakage Current	V_{IN} = 0V	—	—	-10	µA
V_{IH}	High Level Input Voltage		2	—	V_{DD}	V
V_{IL}	Low Level Input Voltage		0	—	0.8	V

LOGIC OUTPUTS

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{OH}	High Level Output Voltage	I_{OH} = -40µA	V_{DD} -0.3	—	—	V
V_{IL}	Low Level Output Voltage	I_{OL} = 1mA, V_{DD} = +5V	—	—	0.4	V
		I_{OL} = 0.4mA, V_{DD} = +3V	—	—	0.4	V

Notes:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

(2) This parameter is tested initially and after a design or process change that affects the parameter.

(3) Latch-up protection is provided for stresses up to 100mA on address and data pins from –1V to V_{CC} + 1V.

POTENTIOMETER CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{REFH} = V_{DD}, V_{REFL} = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
R_{POT}	Potentiometer Resistance	See note 3		24		kΩ
	R_{POT} to RPOT Match		—	±0.5	±1	%
	Pot Resistance Tolerance				±20	%
	Voltage on V_{REFH} pin		2.7		V_{DD}	V
	Voltage on V_{REFL} pin		0		V_{DD} - 2.7	V
	Resolution			0.4		%
INL	Integral Linearity Error			0.5	1	LSB
DNL	Differential Linearity Error			0.25	0.5	LSB
R_{OUT}	Buffer Output Resistance				10	Ω
I_{OUT}	Buffer Output Current				3	mA
TC_{RPOT}	TC of Pot Resistance			300		ppm/ºC
C_H/C_L	Potentiometer Capacitances			8/8		pF

AC ELECTRICAL CHARACTERISTICS

V_{DD} = +2.7V to +5.5V, V_{REFH} = V_{DD}, V_{REFL} = 0V, unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Units
Digital						
t_{CSMIN}	Minimum CS Low Time		150	—	—	ns
t_{CSS}	CS Setup Time		100	—	—	ns
t_{CSH}	CS Hold Time	C_L = 100pF (1)	0	—	—	ns
t_{DIS}	DI Setup Time		50	—	—	ns
t_{DIH}	DI Hold Time		50	—	—	ns
t_{DO1}	Output Delay to 1		—	—	150	ns
t_{DO0}	Output Delay to 0		—	—	150	ns
t_{HZ}	Output Delay to High-Z		—	400	—	ns
t_{LZ}	Output Delay to Low-Z		—	400	—	ns
t_{BUSY}	Erase/Write Cycle Time		—	4	5	ms
t_{PS}	PROG Setup Time		150	—	—	ns
t_{PROG}	Minimum Pulse Width		700	—	—	ns
$t_{CLK}H$	Minimum CLK High Time		500	—	—	ns
$t_{CLK}L$	Minimum CLK Low Time		300	—	—	ns
f_C	Clock Frequency		DC	—	1	MHz
Analog						
t_{DS}	DPP Settling Time to 1 LSB	C_{LOAD} = 10pF, V_{DD} = +5V	—	3	10	µs
		C_{LOAD} = 10pF, V_{DD} = +3V	—	6	10	µs

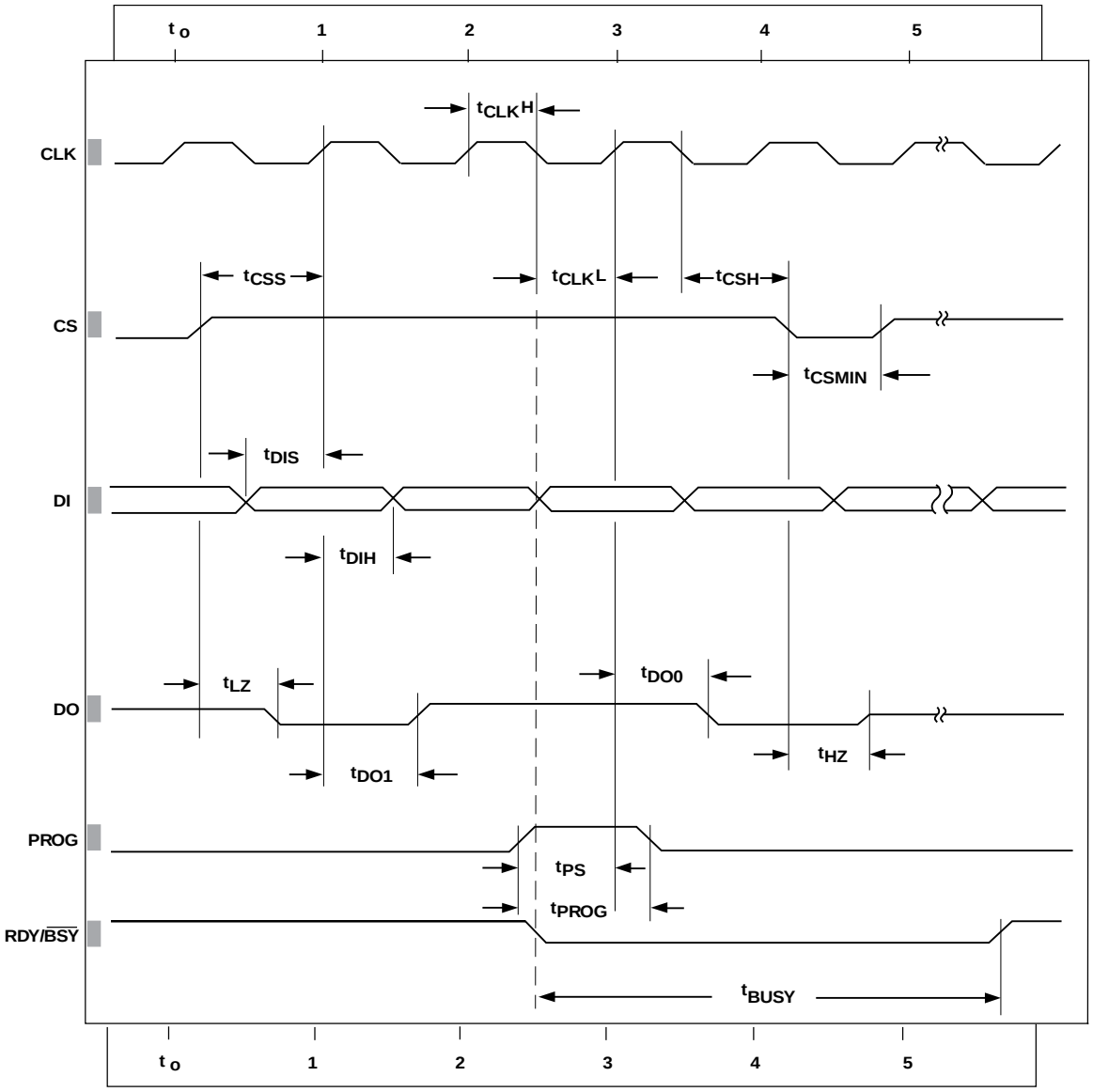
Notes:

(1) All timing measurements are defined at the point of signal crossing V_{DD} / 2.

(2) These parameters are periodically sampled and are not 100% tested.

(3) The 24kΩ +20% resistors are configured as 4 resistors in parallel which would provide a measured value between V_{REFH} and V_{REFL} of 6kΩ +20%. The individual 24kΩ resistors are not measurable but guaranteed by design and verification of the 6kΩ +20% value.

A.C. TIMING DIAGRAM



PIN DESCRIPTION

Pin	Name	Function
1	V_{DD}	Power supply positive
2	CLK	Clock input pin
3	RDY/$\overline{BSY}$	Ready/Busy output
4	CS	Chip select
5	DI	Serial data input pin
6	DO	Serial data output pin
7	PROG	EEPROM Programming Enable Input
8	GND	Power supply ground
9	V_{REFL}	Minimum DAC output voltage
10	NC	No Connect
11	NC	No Connect
12	V_{OUT2}	DPP output channel 2
13	V_{OUT1}	DPP output channel 1
14	V_{REFH}	Maximum DPP output voltage

DPP addressing is as follows:

DPP OUTPUT	A0	A1
V_{OUT1}	0	0
V_{OUT2}	1	0

DEVICE OPERATION

The CAT523 is a dual 8-bit configured digitally programmable potentiometer (DPP) whose outputs can be programmed to any one of 256 individual voltage steps. Once programmed, these output settings are retained in non-volatile memory and will not be lost when power is removed from the chip. Upon power up the DPPs return to the settings stored in non-volatile memory. Each DPP can be written to and read from independently without effecting the output voltage during the read or write cycle. Each output can also be temporarily adjusted without changing the stored output setting, which is useful for testing new output settings before storing them in memory.

DIGITAL INTERFACE

The CAT523 employs a 3 wire, Microwire-like, serial control interface consisting of Clock (CLK), Chip Select (CS) and Data In (DI) inputs. For all ope–rations, address and data are shifted in LSB first. In addition, all digital data must be preceded by a logic "1" as a start bit. The DPP address and data are clocked into the DI pin on the clock's rising edge. When sending multiple blocks of information a minimum of two clock cycles is required between the last block sent and the next start bit.

Multiple devices may share a common input data line by selectively activating the CS control of the desired IC. Data Outputs (DO) can also share a common line because the DO pin is Tri-Stated and returns to a high impedance when not in use.

CHIP SELECT

Chip Select (CS) enables and disables the CAT523's read and write operations. When CS is high data may be read to or from the chip, and the Data Output (DO) pin is active. Data loaded into the DPP control registers will remain in effect until CS goes low. Bringing CS to a logic low returns all DPP outputs to the settings stored in non-volatile memory and switches DO to its high impedance Tri-State mode.

Because CS functions like a reset the CS pin has been equipped with a 30 ns to 90 ns filter circuit to prevent noise spikes from causing unwanted resets and the loss of volatile data.

CLOCK

The CAT523's clock controls both data flow in and out of the IC and non-volatile memory cell programming. Serial data is shifted into the DI pin and out of the DO pin on the clock's rising edge. While it is not necessary for the clock to be running between data transfers, the clock must be operating in order to write to non-volatile memory, even though the data being saved may already be resident in the DPP wiper control register.

No clock is necessary upon system power-up. The CAT523's internal power-on reset circuitry loads data from non-volatile memory to the DPPs without using the external clock.

As data transfers are edge triggered clean clock transitions are necessary to avoid falsely clocking data into the control registers. Standard CMOS and TTL logic families work well in this regard and it is recommended that any mechanical switches used for breadboarding or device evaluation purposes be debounced by a flip-flop or other suitable debouncing circuit.

V_{REF}

V_{REF}, the voltage applied between pins V_{REFH} & V_{REFL}, sets the DPP's Zero to Full Scale output range where V_{REFL} = Zero and V_{REFH} = Full Scale. V_{REF} can span the full power supply range or just a fraction of it. In typical applications V_{REFH} & V_{REFL} are connected across the power supply rails. When using less than the full supply voltage V_{REFH} is restricted to voltages between V_{DD} and $V_{DD}/2$ and V_{REFL} to voltages between GND and $V_{DD}/2$.

READY/$\overline{\text{BUSY}}$

When saving data to non-volatile memory, the Ready/Busy output (RDY/$\overline{\text{BSY}}$) signals the start and duration of the non-volatile erase/write cycle. Upon receiving a command to store data (PROG goes high) RDY/$\overline{\text{BSY}}$ goes low and remains low until the programming cycle is complete. During this time the CAT523 will ignore any data appearing at DI and no data will be output on DO.

RDY/$\overline{\text{BSY}}$ is internally ANDed with a low voltage detector circuit monitoring V_{DD}. If V_{DD} is below the minimum value required for non-volatile programming, RDY/$\overline{\text{BSY}}$ will remain high following the program command indicating a failure to record the desired data in non-volatile memory.

DATA OUTPUT

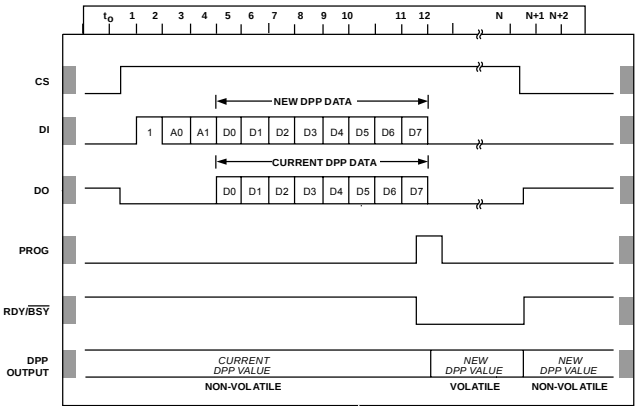
Data is output serially by the CAT523, LSB first, via the Data Out (DO) pin following the reception of a start bit and two address bits by the Data Input (DI). DO becomes active whenever CS goes high and resumes its high impedance Tri-State mode when CS returns low. Tri-Stating the DO pin allows several 523s to share a single serial data line and simplifies interfacing multiple 523s to a microprocessor.

WRITING TO MEMORY

Programming the CAT523's non-volatile memory is accomplished through the control signals: Chip Select (CS) and Program (PROG). With CS high, a start bitfollowed by a two bit DPP address and eight data bits are clocked into the DPP control register via the DI pin. Data enters on the clock's rising edge. The DPP output changes to its new setting on the clock cycle following D7, the last data bit.

Programming is achieved by bringing PROG high sometime after the start bit and at least 150 ns prior to the rising edge of the clock cycle immediately following the D7 bit. Two clock cycles after the D7 bit the DAC control register will be ready to receive the next set of address and data bits. The clock must be kept running throughout the programming cycle. Internal control circuitry takes care of ramping the programming voltage for data transfer to the non-volatile memory cells. The CAT523's non-volatile memory cells will endure over 100,000 write cycles and will retain data for a minimum of 100 years without being refreshed.

Figure 1. Writing to Memory



READING DATA

Each time data is transferred into a DPP wiper control register currently held data is shifted out via the D0 pin, thus in every data transaction a read cycle occurs. Note, however, that the reading process is destructive. Data must be removed from the register in order to be read. Figure 2 depicts a Read Only cycle in which no change occurs in the DPP's output. This feature allows µPs to poll DPPs for their current setting without disturbing the output voltage but it assumes that the setting being read is also stored in non-volatile memory so that it can be restored at the end of the read cycle. In Figure 2 CS returns low before the 13th clock cycle completes. In doing so the non-volatile memory setting is reloaded into the DPP wiper control register.

Since this value is the same as that which had been there previously no change in the DPP's output is noticed. Had the value held in the control register been different from that stored in non-volatile memory then *a change would occur* at the read cycle's conclusion.

TEMPORARILY CHANGE OUTPUT

The CAT523 allows temporary changes in DPP's output to be made without disturbing the settings retained in non-volatile memory. This feature is particularly useful when testing for a new output setting and allows for user adjustment of preset or default values without losing the original factory settings.

Figure 3 shows the control and data signals needed to effect a temporary output change. DPP wiper settings may be changed as many times as required and can be made to any of the two DPPs in any order or sequence. The temporary setting(s) remain in effect long as CS remains high. When CS returns low all two DPPs will return to the output values stored in non-volatile memory.

When it is desired to save a new setting acquired using this feature, the new value must be reloaded into the DPP wiper control register prior to programming. This is because the CAT523's internal control circuitry discards the new data from the programming register two clock cycles after receiving it (after reception is complete) if no PROG signal is received.

Figure 2. Reading from Memory

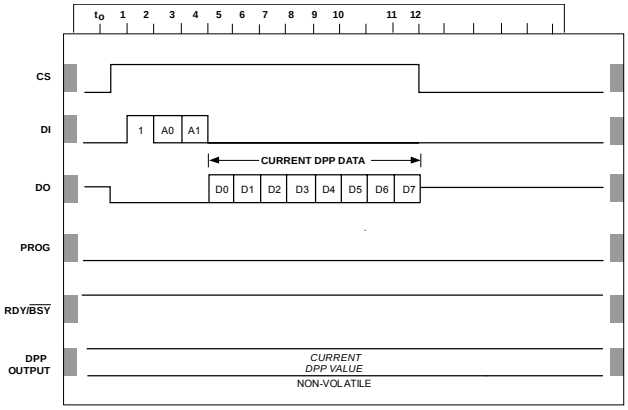
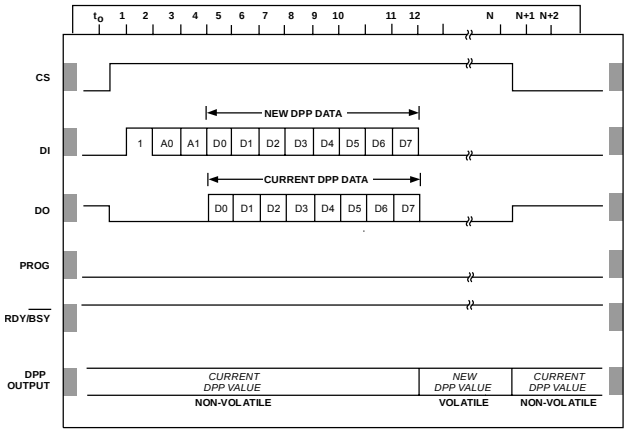
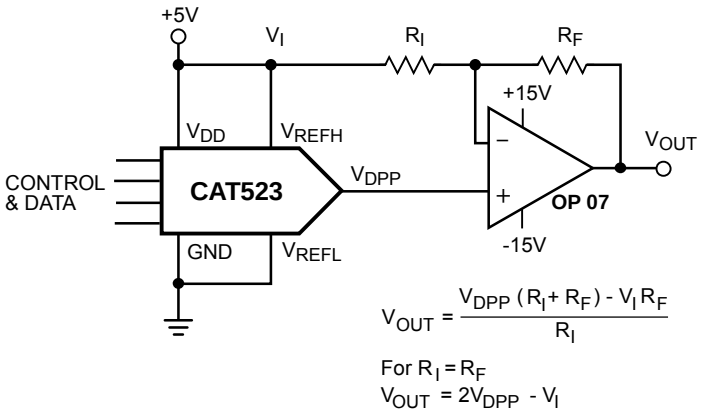


Figure 3. Temporary Change in Output



APPLICATION CIRCUITS



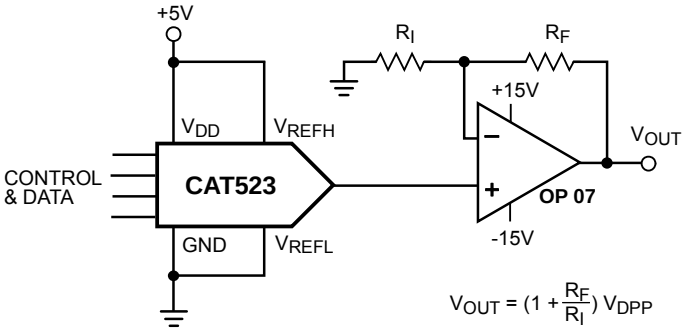
$$V_{OUT} = \frac{V_{DPP}(R_I + R_F) - V_I R_F}{R_I}$$

For $R_I = R_F$

$V_{OUT} = 2V_{DPP} - V_I$

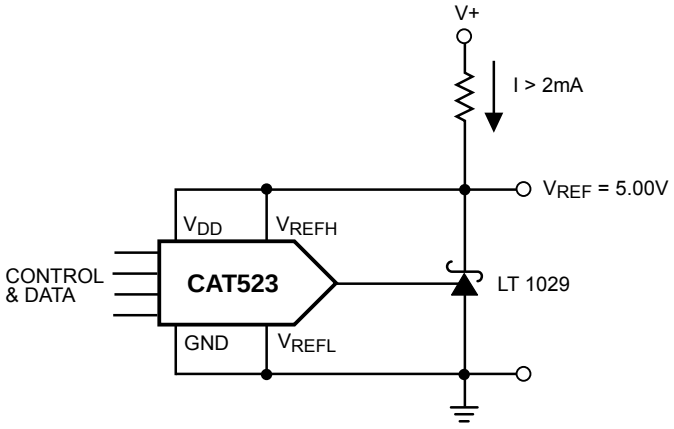
DPP INPUT		DPP OUTPUT	ANALOG OUTPUT
MSB	LSB	$V_{DPP} = \frac{CODE}{255} \times (V_{FS} - V_{ZERO}) + V_{ZERO}$	
		$V_{FS} = 0.99V_{REF}$	$V_{REF} = 5V$
		$V_{ZERO} = 0.01V_{REF}$	$R_I = R_F$
1111	1111	$\frac{255}{255} \times 0.98V_{REF} + 0.01V_{REF} = 0.990V_{REF}$	$V_{OUT} = +4.90V$
1000	0000	$\frac{128}{255} \times 0.98V_{REF} + 0.01V_{REF} = 0.502V_{REF}$	$V_{OUT} = +0.02V$
0111	1111	$\frac{127}{255} \times 0.98V_{REF} + 0.01V_{REF} = 0.498V_{REF}$	$V_{OUT} = -0.02V$
0000	0001	$\frac{1}{255} \times 0.98V_{REF} + 0.01V_{REF} = 0.014V_{REF}$	$V_{OUT} = -4.86V$
0000	0000	$\frac{0}{255} \times 0.98V_{REF} + 0.01V_{REF} = 0.010V_{REF}$	$V_{OUT} = -4.90V$

Bipolar DPP Output

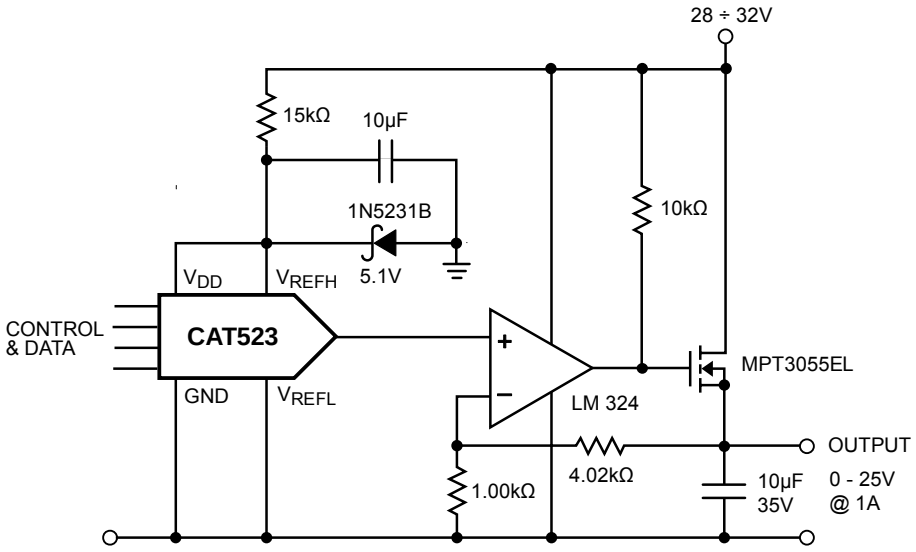


$$V_{OUT} = (1 + \frac{R_F}{R_I})\, V_{DPP}$$

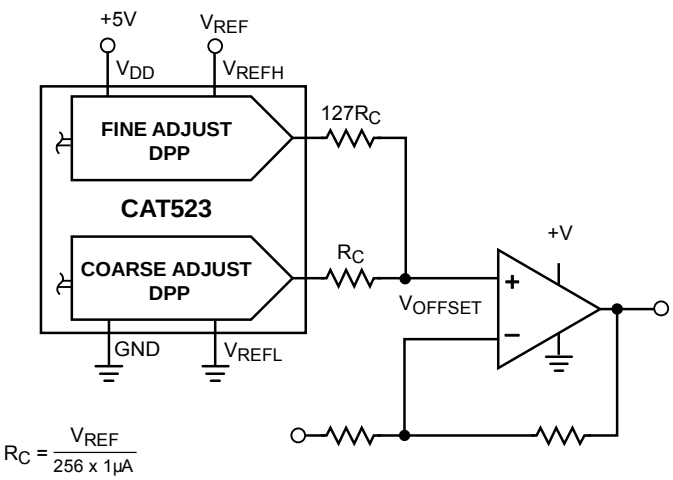
Amplified DPP Output



Digitally Trimmed Voltage Reference



Digitally Controlled Voltage Reference

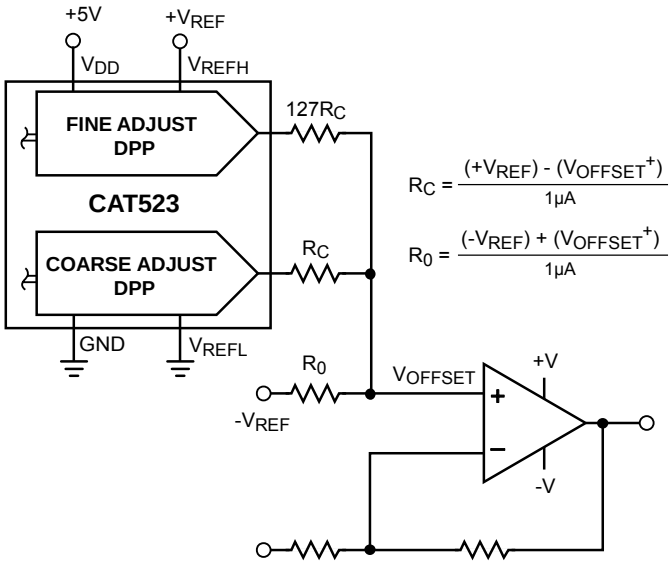


$$R_C = \frac{V_{REF}}{256 \times 1\mu A}$$

Fine adjust gives ±1 LSB change in V_{OFFSET}

when $V_{OFFSET} = V_{REF}/2$

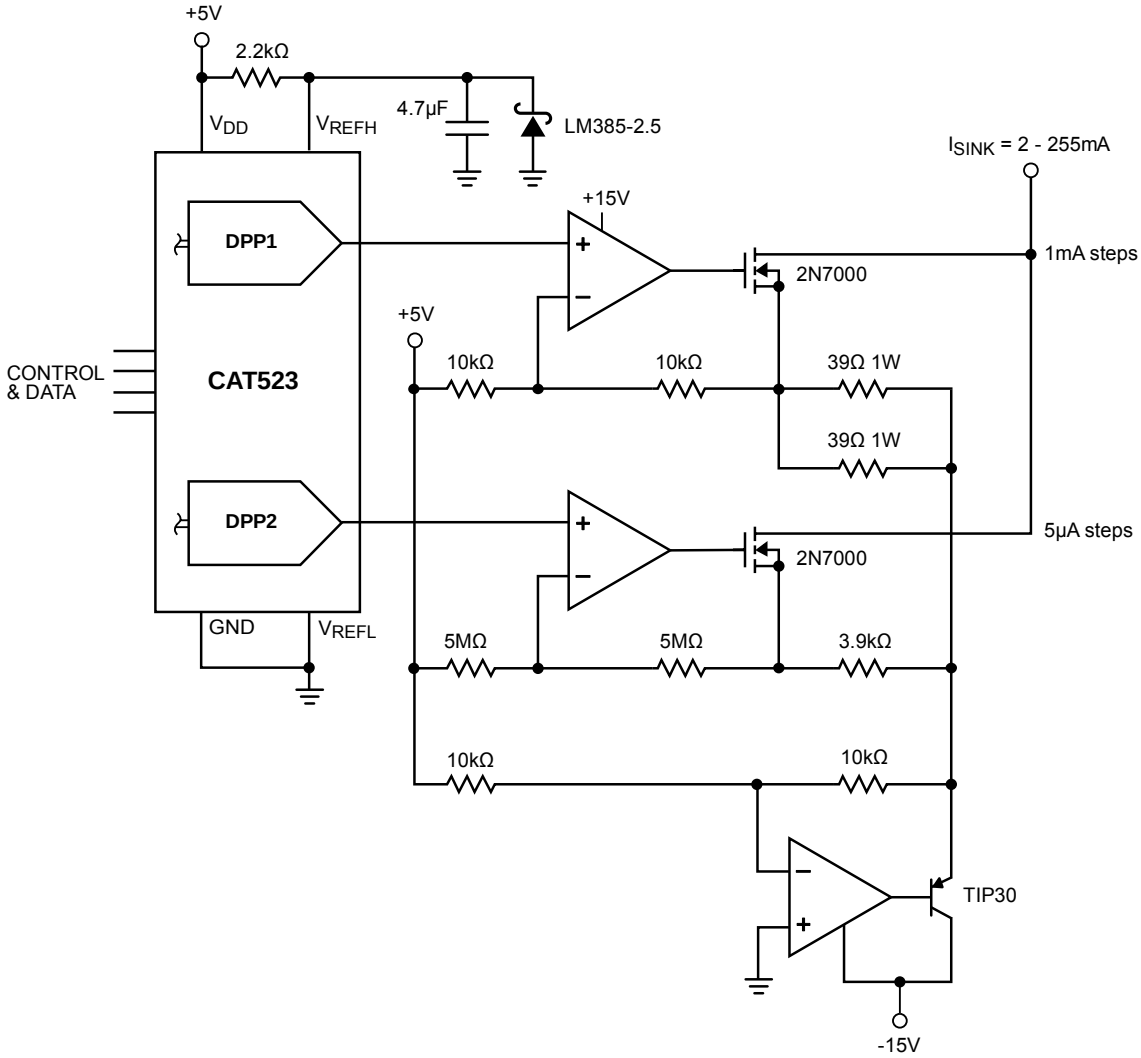
Coarse-Fine Offset Control by Averaging DPP Outputs for Single Power Supply Systems



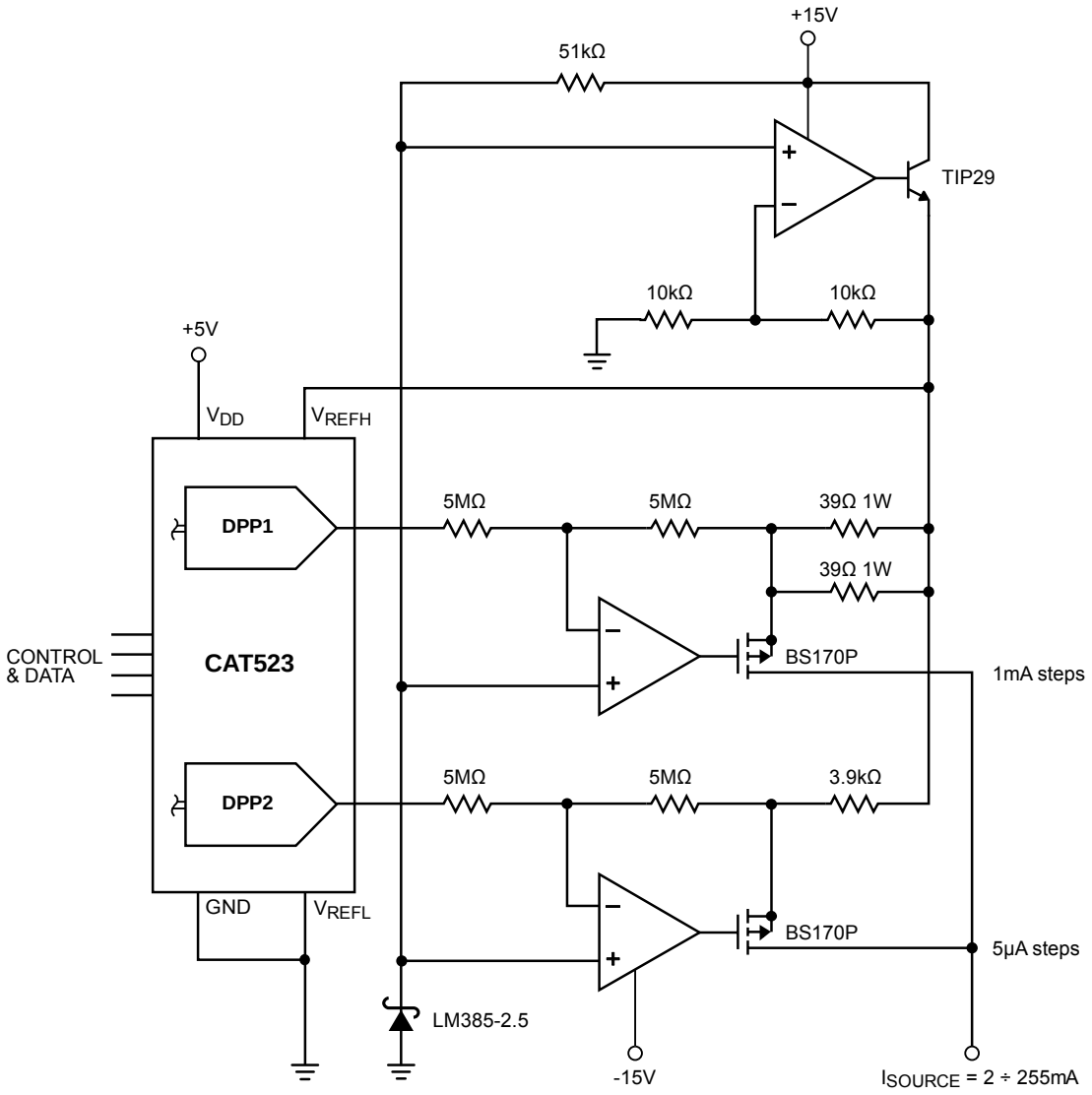
$$R_C = \frac{(+V_{REF}) - (V_{OFFSET}^{+})}{1\mu A}$$

$$R_0 = \frac{(-V_{REF}) + (V_{OFFSET}^{+})}{1\mu A}$$

Coarse-Fine Offset Control by Averaging DPP Outputs for Dual Power Supply Systems



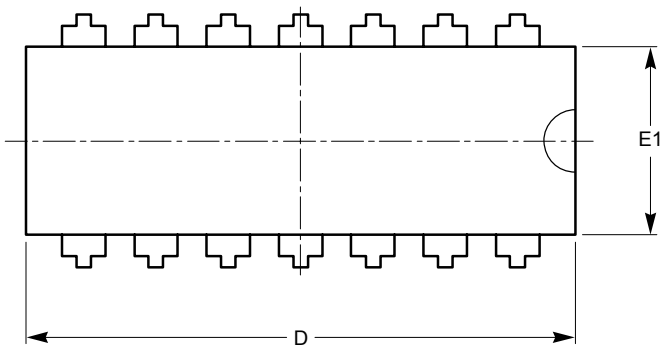
Current Sink with 4 Decades of Resolution



Current Source with 4 Decades of Resolution

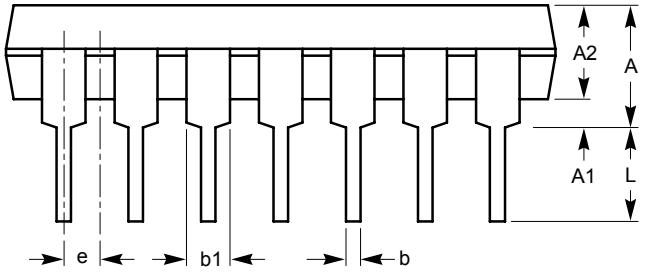
PACKAGE OUTLINE DRAWINGS

PDIP 14-Lead (L)[1][2]

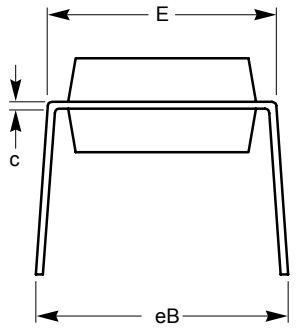


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	3.56		5.33
A1	0.38		
A2	2.92	3.30	4.95
b	0.36	0.45	0.55
b1	1.15	1.52	1.77
c	0.21	0.26	0.35
D	18.67	19.05	19.68
E	7.62	7.87	8.25
E1	6.10	6.35	7.11
e		2.54 BSC	
eB	7.88		10.92
L	2.99	3.30	3.81



SIDE VIEW

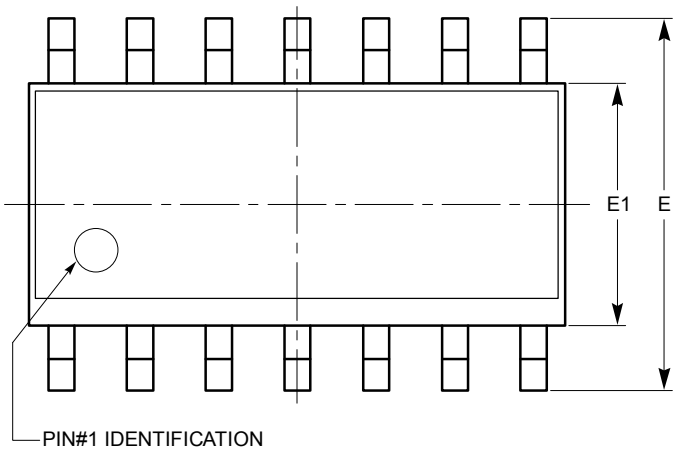


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

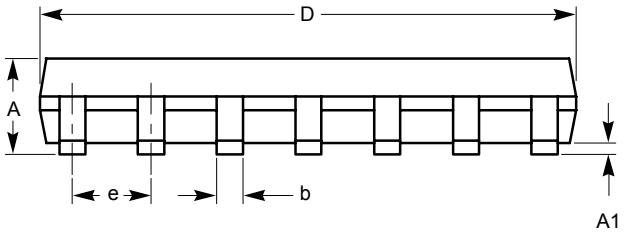
Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MS-001.

SOIC 14-Lead (W)[1][2]

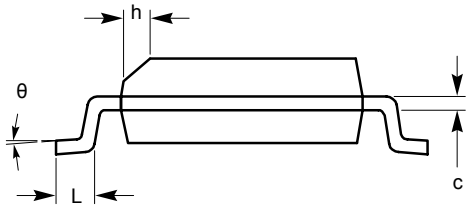


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	8.55	8.65	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW

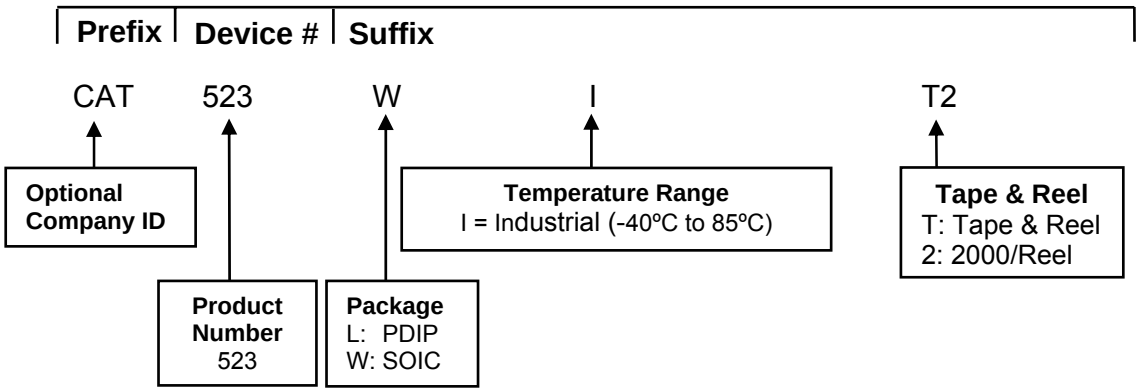


END VIEW

For current Tape and Reel information, download the PDF file from: http://www.catsemi.com/documents/tapeandreel.pdf.

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC standard MS-012.

EXAMPLE OF ORDERING INFORMATION



Notes:

(1) All packages are RoHS compliant (Lead-free, Halogen-free).
(2) Standard lead finish is Matte-Tin.
(3) This device used in the above example is a CAT523WI-T2 (SOIC, Industrial Temperature, Tape & Reel).

ORDERING PART NUMBER

CAT523LI
CAT523WI

REVISION HISTORY

Date	Revision	Description
16-Mar-04	D	Updated Potentiometer Characteristics
12-Jul-04	E	Updated Functional Diagram Updated Potentiometer Characteristics Added Note 3 under Potentiometer/AC Characteristics tables
26-Jul-07	F	Add Package Outline Drawings Updated Example of Ordering Information Added MD- to document number
08-Oct-07	G	Change title Update Writing to Memory
15-Jul-08	H	Add “Not Recommended for New Design” to the top of all pages

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